香港中文大學
The Chinese University of Hong Kong

CENG3430 Rapid Prototyping of Digital Systems

Lecture 00: Course Information

Ming-Chang YANG

mcyang@cse.cuhk.edu.hk

CENG3430 Course Information

- **CENG3430 Rapid Prototyping of Digital Systems**
- **Course Time and Place**
  - **Lecture** (*2)
    - MON 16:30~18:15 (@MMW 710)
  - **Lab** (*2)
    - TUE 16:30~18:15 (@SHB 102)
    - Note: It's required to attend both lab sessions.
- **Course Website**
  - http://www.cse.cuhk.edu.hk/~mcyang/ceng3430/2122T2/ceng3430.html
  - https://blackboard.cuhk.edu.hk/

Course Instructor & Teaching Assistants

- **Course Instructor**
  - Prof. Ming-Chang YANG (楊明昌)
    - Office: **ZOOM**
    - Office Hours: *Requested by email*
    - Email: mcyang@cse.cuhk.edu.hk
- **Teaching Assistants**
  - Chao WANG (王超)
    - Office: **ZOOM**
    - Office Hours: WED 15:30~16:30
    - Email: cwang@cse.cuhk.edu.hk
  - Lok Yin CHOW (周樂言)
    - Office: **ZOOM**
    - Office Hours: THUR 15:00~16:00
    - Email: lychow@cse.cuhk.edu.hk

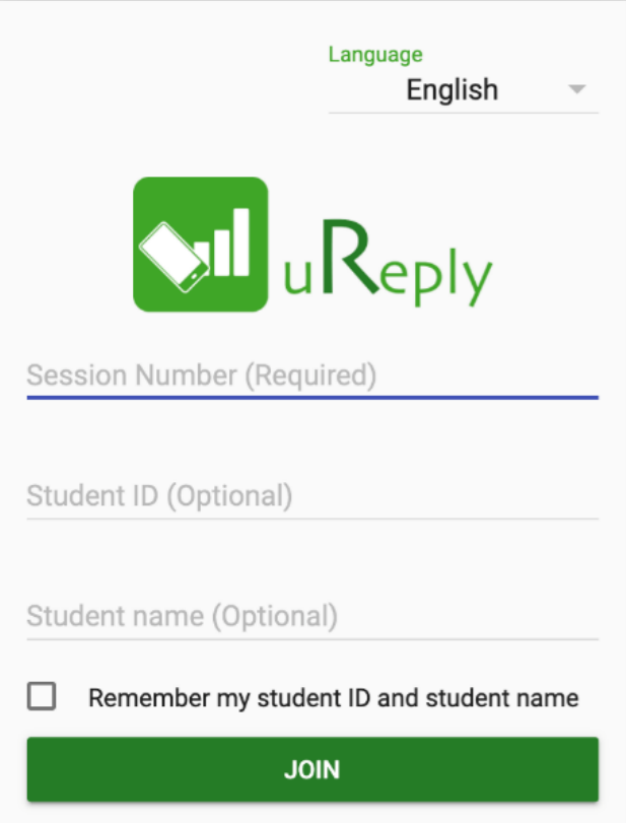
Course Assessment

- **Grading** *(subject to changes)*
  - Class Participation 10%
  - Weekly Lab Exercises 40%
  - Final Project 50%
  - Bonus 5% (be active!)

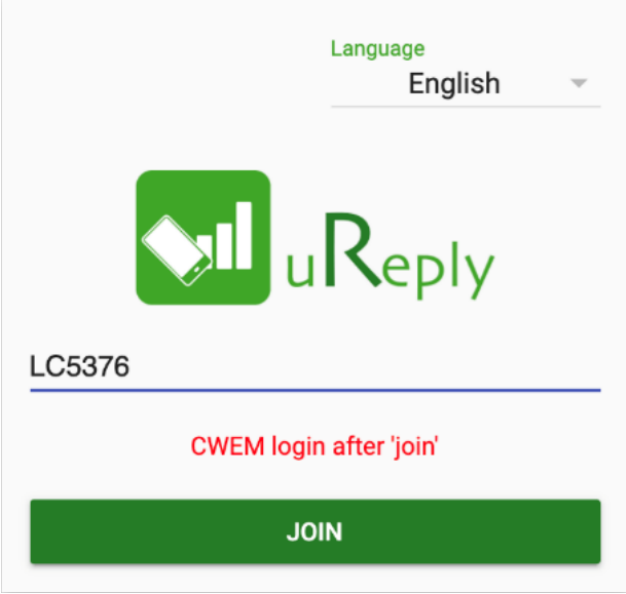
- **Notes**
  - Weekly Lab Exercises: Individual
  - Final project: At most two students in a group
  - Late submission is NOT acceptable (unless otherwise approved before the regular deadline)

uReply: Enter the Session

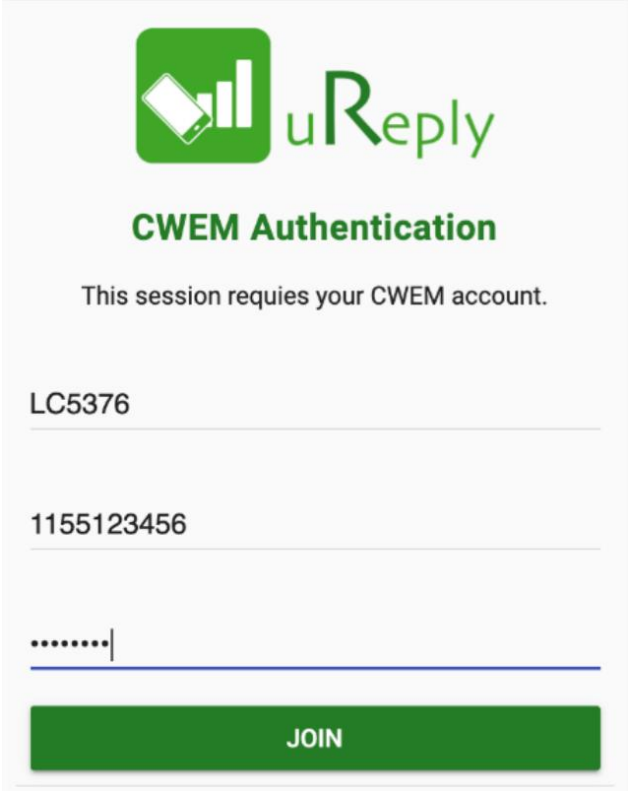
1) Enter the Session Number



2) Confirm the Session Number and Click "Join"



3) Login with Student ID and CWEM Password

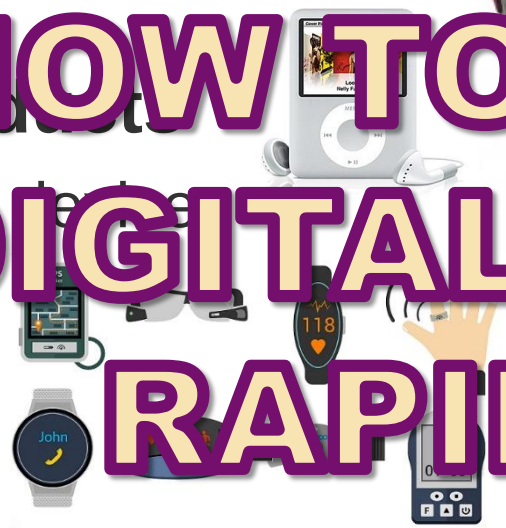


uReply Attendance User Guide

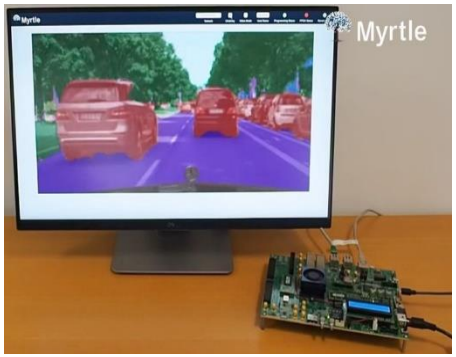
We Are Surrounded by Digital Systems

- **Mass Products**
  - Media players
  - Mobile phones

- **Novel Products**
  - Wearable devices
  - Robots



- **Research**
  - Real time edge detection
  - Deep learning acceleration



HOW TO BUILD A DIGITAL SYSTEM RAPIDLY?

Common Design Flow of Digital System

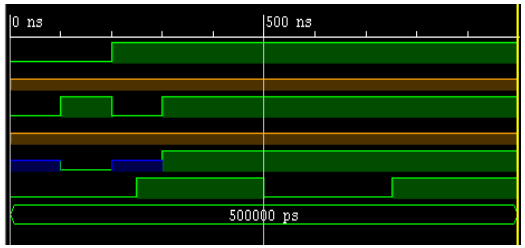
Idea Generation

Drafting on Paper

Designing Chip (VHDL)

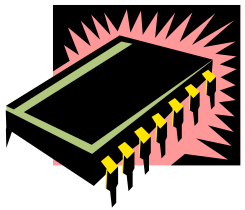
Ex: VHDL AND-Gate Program

```
1 entity and2 is
2 port (a,b: in std_logic;
3         c: out std_logic);
4 end and2
5 architecture arch of and2
6 begin
7    c <= a and b;
8 end and2_arch
```



Testing (FPGA)

Manufacturing
Production Line Design



Quality Control

Our Focus: Prototyping

Idea Generation

Drafting on Paper

Designing Chip (VHDL)

Ex: VHDL AND-Gate Program

```
1 entity and2 is
2 port (a,b: in std_logic;
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4 end and2
5 architecture arch of and2
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```
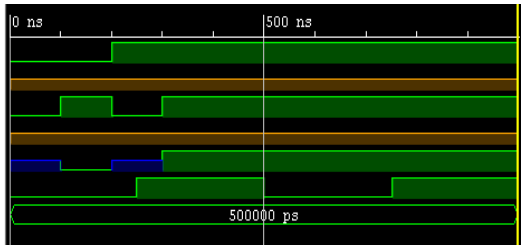
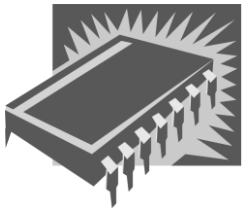



Testing (FPGA)

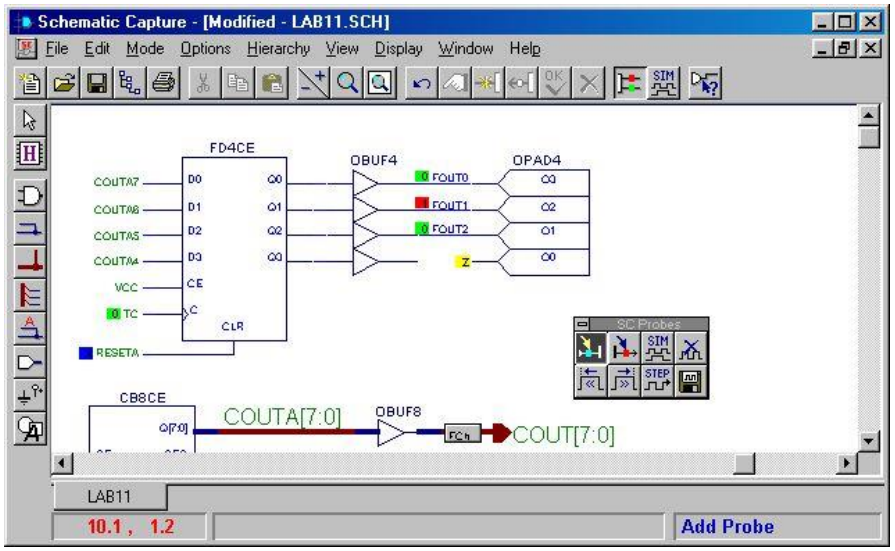
Manufacturing
Production Line Design



Quality Control

Methods for Digital System Design

- **Schematic Method**
  - Complicated
  - Suitable for top level design to merge modules
    - Like data flow block diagram



- **Programming Language**
  - VHDL (**V**ery-High-Speed-Integrated-Circuits **H**ardware **D**escription **L**anguage)
    - Each module in the schematic can be implemented by VHDL.
  - Verilog

Ex: VHDL AND-Gate Program

```
1 entity and2 is
2 port (a,b: in std_logic;
3         c: out std_logic);
4 end and2
5 architecture and2_arch of and2
6 begin
7    c <= a and b;
8 end and2_arch
```

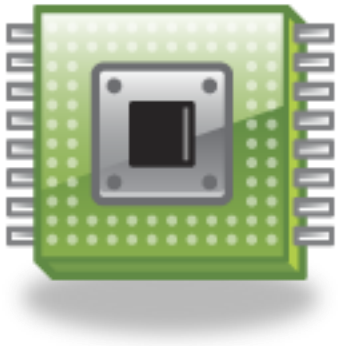
What We Will Learn: HDL + FPGA

- **Software**: Hardware Description Language (HDL)

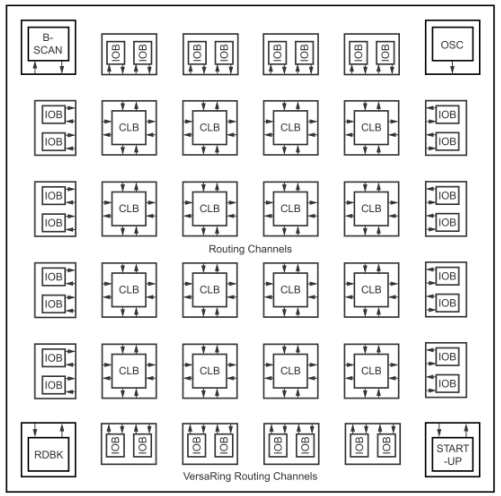
Ex: VHDL AND-Gate Program

```
1 entity and2 is
2 port (a,b: in std_logic;
3         c: out std_logic);
4 end and2
5 architecture and2_arch of and2
6 begin
7    c <= a and b;
8 end and2_arch
```

Write HDL code, then it will generate the hardware chip automatically

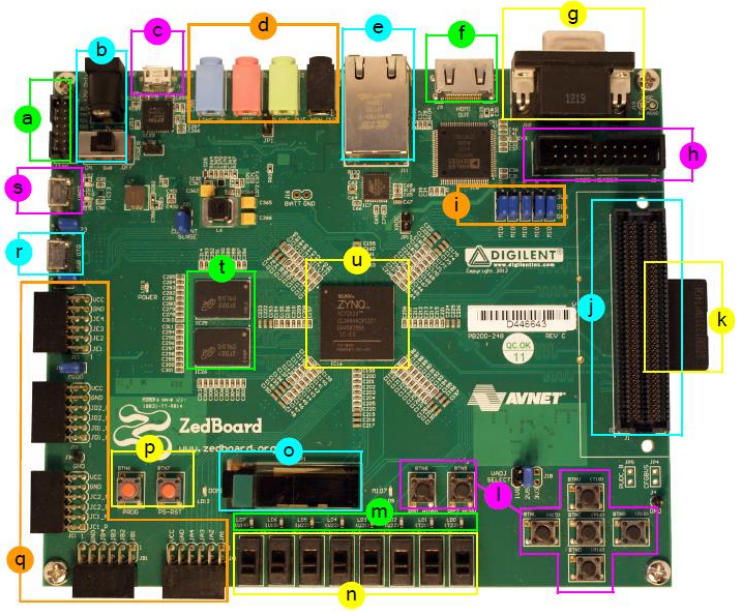


- **Hardware**: Field Programmable Gate Array (FPGA)
  - The hardware can be reprogrammable.
  - Designs can be changed easily.
  - No additional hardware manufacturing cost is needed.



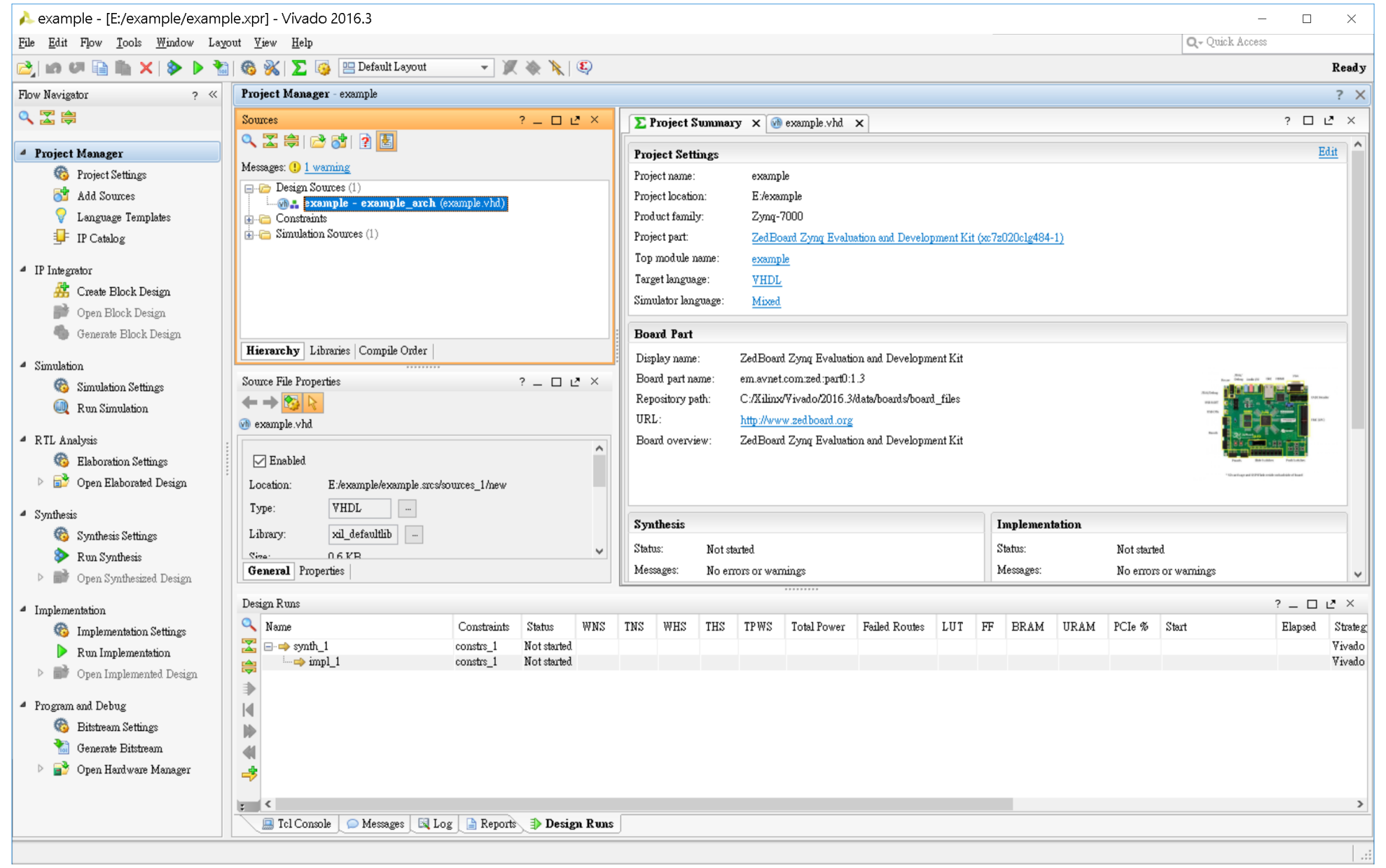
What We Will Use in Our Lab

- **Software**: Vivado WebPACK™ Edition (FREE)
  - It supports Windows or Linux operating systems.
  - **Hardware Description Language**: Very-High-Speed-Integrated-Circuits Hardware Description Language (**VHDL**)
- **Hardware**: Zynq ZedBoard
  - Dual-core ARM Cortex-A9 with traditional FPGA



a Xilinx JTAG connector
b Power input and switch
c USB-JTAG (programming)
d Audio ports
e Ethernet port
f HDMI port (output)
g VGA port
h XADC header port
i Configuration jumpers
j FMC connector
k SD card (underside)
l User push buttons
m LEDs
n Switches
o OLED display
p Prog & reset push buttons
q 5 x Pmod connector ports
r USB-OTG peripheral port
s USB-UART port
t DDR3 memory
u Zynq device (+ heatsink)

Software: Vivado WebPACK™ Edition



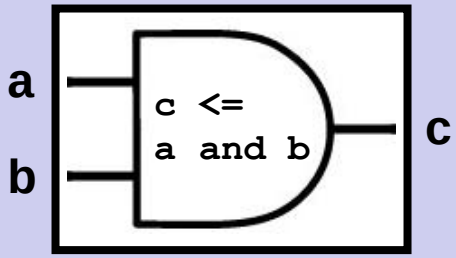
Hardware Description Language: VHDL

- **An Example: AND-Gate in VHDL**

Entity Declaration: Define I/Os

```
1 entity and2 is
2 port (a,b: in std_logic;
3           c: out std_logic);
4 end and2
```

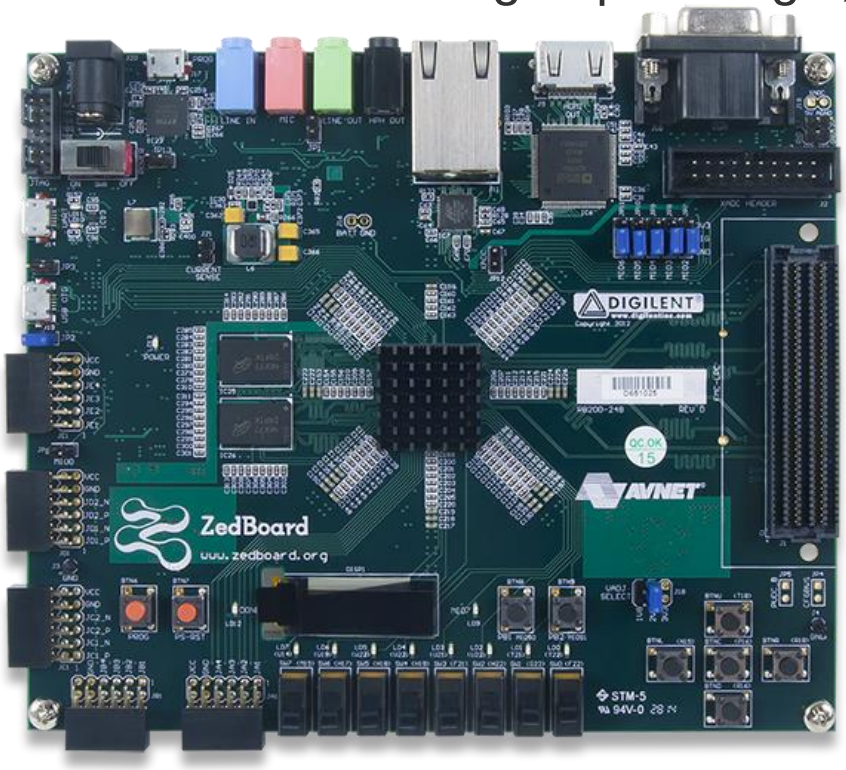
```
5 architecture and2_arch of and2
6 begin
7     c <= a and b;
8 end and2_arch
```

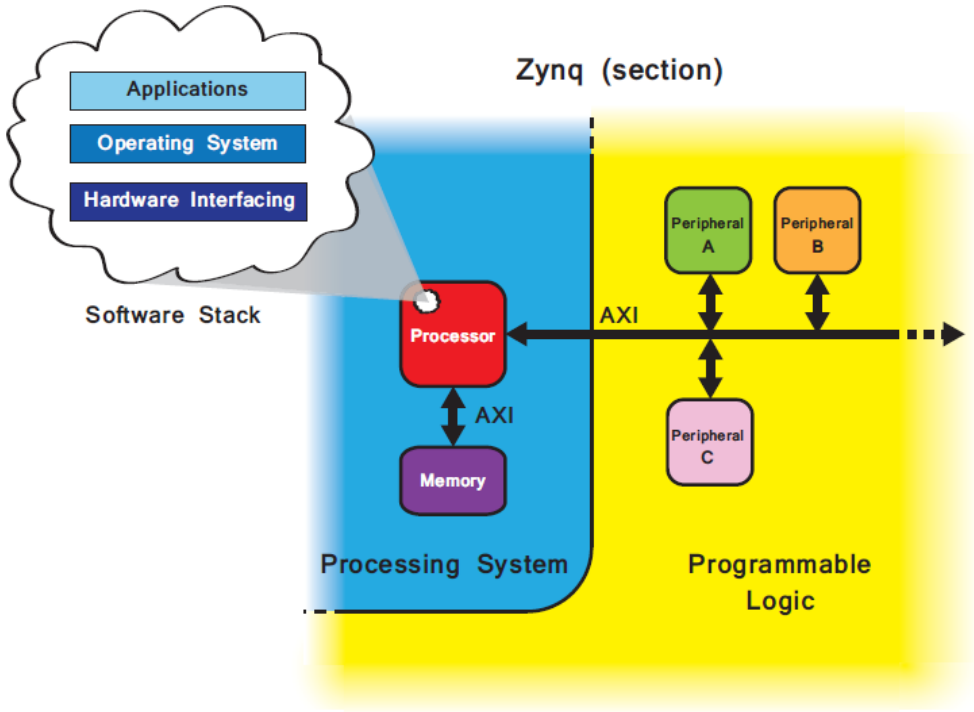


Architecture Body: Define functions

Hardware: Zynq ZedBoard

- Zynq ZedBoard combines
  - Processing System (PS): Dual-core ARM Cortex-A9 CPU
    - Supports software routines and/or operating systems
  - Programmable Logical (PL): Equivalent to trad. FPGA
    - Ideal for high-speed logic, arithmetic and data flow subsystems





Course Schedule *(subject to change)*

W	Date	Lecture	Lab
1	Jan 10, 11	Lec00: Course Information	No Lab
2	Jan 17, 18	Lec01: Introduction to VHDL	Lab01: Vivado & Software Simulation
3	Jan 24, 25	Lec02: Introduction to ZedBoard	Lab02: First Program on ZedBoard
4	Jan 31, Feb 1	Lunar New Year Vacation (No Class)	Lunar New Year Vacation (No Lab)
5	Feb 7, 8	Lec03: Comb. Circuit and Seq. Circuit	Lab03: Serial-in-parallel-out Shift Register
6	Feb 14, 15	Lec04: Driving Clock and Pmod	Lab04: Driving Seven Segment Display
7	Feb 21, 22	Lec05: Driving VGA Display	Lab05: Driving VGA Display
8	Feb 28, Mar 1	Lec06: Communication Protocols	Lab06: Driving SPI/I2C Pmod
9	Mar 7, 8	Lec07: Integration of ARM and FPGA	Lab07: Software Stopwatch
10	Mar 14, 15	Lec08: Embedded Operating System	Lab08: Software Stopwatch with Linux
11	Mar 21, 22	Lec09: High Level Synthesis	Lab09: High Level Synthesis Exercise
12	Mar 28, 29	Final Project Proposal	Final Project Proposal Feedback
13	Apr 4, 5	Reading Week (No Class)	Public Holiday (No Lab)
14	Apr 11, 12	Lec10: Introduction to Verilog	Lab10: Verilog Exercise
15	Apr 18, 19	Public Holiday (No Class)	Final Project Progress Report
	May ?? (TBA)	Final Project Submission Deadline	

Full Final Project List (2020-21)

1. Digital Locker
2. Weather Report Generation
3. Reaction Game
4. Snake Game
5. Audition (Rhythm Game)
6. Kernel Convolution
7. GOMOKU
8. Football Shooting Game
9. Catch the Thief
10. The Snake Game
11. FLAPPY BIRD
12. Mota Game
13. Flappy Bird
14. Snake Game

Full Final Project List (2019-20)

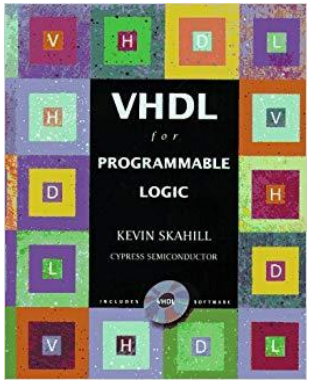
1. AVG Game
2. Door Locking System
3. The Flappy Bird
4. Immigration System
5. Traffic Horn Punishment
6. How Fast Is Your Finger
7. Mastermind
8. Drum Looper
9. Gobang
10. Morse Code from Torch
11. Indoor Monitoring Station
12. Rhythm Game
13. Cat Dog Fight Game
14. Portable Freezer
15. Color Detector
16. Mastermind
17. Tic Tac Toe
18. UFO Catcher
19. Sound Recorder

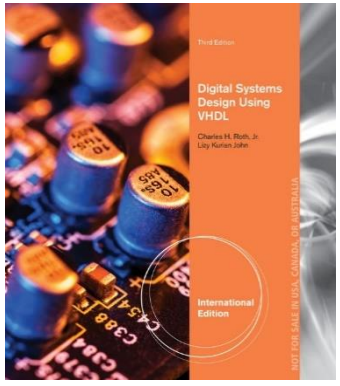
Full Final Project List (2018-19)

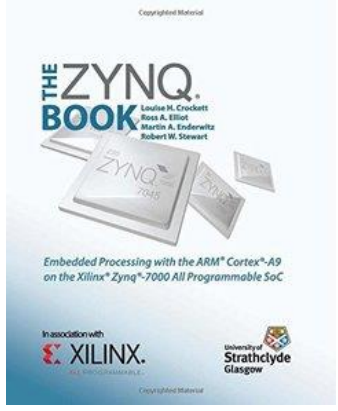
1. Piano and Music Player
2. Color Recognition
3. RGB Meter
4. Lie Detector
5. Snake Battle
6. Space War
7. The Dodge Game
8. Space Impact
9. Get It at Once
10. Elevator
11. Super Pads
12. Tetris
13. Morse Code Interpreter
14. The Flash
15. Multifunctional Display
16. Rolling Down!

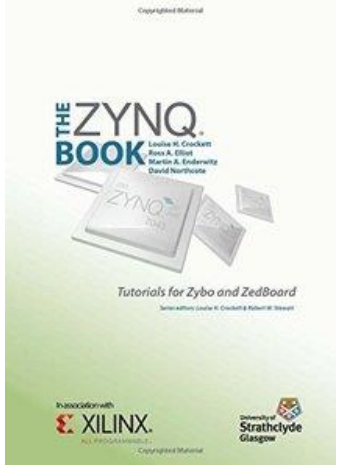
References

- **VHDL for Programmable Logic**
  - Kevin Skahill
  - Addison-Wesley
- **Digital Systems Design Using VHDL**
  - Charles H. Roth Jr., Lizy Kurian John
  - Cengage Learning
- **The Zynq Book**: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc
  - Louise H Crockett, Ross A Elliot, Martin A Enderwitz, Robert W Stewart
  - Strathclyde Academic Media
- **The Zynq Book**: Tutorials for Zybo and ZedBoard
  - Louise H Crockett, Ross A Elliot, Martin A Enderwitz
  - Strathclyde Academic Media









Important Notes

- Visit our course website regularly!

- Plagiarism will **NOT** be tolerated!
  - Don't copy!
  - Don't let other(s) copy!
  - Can discuss but write up the solutions by yourself!

- Honesty in Academic Work:
  - http://www.cuhk.edu.hk/policy/academichonesty/

The best way to learn is through practice!

Severe Penalties on Dishonesty (1/3)

(iii)	Employing or using services provided by a third party [Note 1] to undertake the examinations/ final year projects/ papers/ essays/ dissertations, or providing services as a third party, including any one of the following aspects: (a) employing or using services provided by a third party; (b) providing services as a third party; (c). sharing of any materials obtained from the employment or use of services provided by a third party to other students; and (d) knowingly using materials obtained by anyone who has employed or used the services provided by a third party.	(i)	three demerits (of which one will remain in the University's record permanently and two are reviewable);
		(ii)	a failure grade for the course concerned (not applicable to the student who is the third party to provide the services but not taking the same course or not taking it in the same term);
		(iii)	suspension from the University for one term [Note 2]; and
		(iv)	lowering the degree classification by one level upon graduation (not applicable to undergraduate students who graduate with a Pass Degree, MBChB students and postgraduate students) [Note 3].
(v)	Distribution/ Sharing/ Copying of teaching materials without the consent of the course teachers to gain unfair academic advantage in the courses	(i)	two demerits.

Severe Penalties on Dishonesty (2/3)

(vi)	Violating rule 15 or 16 of the University's Examination Rules (Annex 1) or rule 9 or 10 of the University's Online Examination Rules (Annex 2)	First offence	
		(i)	one demerit.
		Second or further offence (and a first offence that is serious as decided by the disciplinary committee concerned/the FTP Committee)	
		(i)	two demerits (of which one will remain in the University's record permanently and one is reviewable).
(vii)	Cheating in tests and examinations (including violation of rule 17 or 18 of the University's Examination Rules or rule 11, 12, 13, 14 or 16 of the University's Online Examination Rules)	First offence	
		(i)	one demerit (which will remain in the University's record permanently); and
		(ii)	a failure grade for the course concerned.
		Second or further offence (and a first offence that is serious as decided by the disciplinary committee concerned/the FTP Committee)	
		(i)	two demerits (of which one will remain in the University's record permanently and one is reviewable); and
		(ii)	a failure grade for the course concerned.

Severe Penalties on Dishonesty (3/3)

(viii)	Impersonation fraud in tests and examinations (including violation of rule 19 of the University's Examination Rules or rule 15 of the University's Online Examination Rules)	(i)	three demerits (of which one will remain in the University's record permanently and two are reviewable);
		(ii)	a failure grade for the course concerned;
		(iii)	suspension from the University for one term [Note 1]; and
		(iv)	lowering the degree classification by one level upon graduation (not applicable to undergraduate students who graduate with a Pass Degree, MBChB students and postgraduate students) [Note 2].
		[The same penalties apply to the student who asks/allows someone to assume his/her identity to sit for a test/an examination as well as to the student who sits for a test/an examination if both parties are students of the University, except that penalty (ii) will not apply to the latter.]	